

IN THE CLAIMS

Please amend claims 1-3, 5-9, and 14-17 as follows. All claims have been provided as a courtesy to the Examiner.

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1. (Amended) A memory module, comprising:  
2 a plurality of memory devices; and  
3 a memory module controller configured to receive a first memory transaction  
4 in a first format from a first memory bus, and [to control] to convert the first memory  
5 transaction into a second memory transaction in a second format [access to] for  
6 the plurality of memory devices, the second format of the second memory  
7 transaction being different from the first format of the first memory transaction.

1 2. (Amended) The memory module of claim 1, wherein the memory module  
2 controller is also configured to reformat [receives] the first memory transaction in  
3 [a] the first format [, and reformats the first memory transaction] into [a] the second  
4 memory transaction in the second format, and [the memory module controller  
5 providing] to provide the [reformatted] second memory transaction to at least one  
6 of the plurality of memory devices.

1 3. (Amended) The memory module of claim 1, further comprising:  
2 a second memory bus coupled between the memory module controller and  
3 the plurality of memory devices.

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1 4. (Unchanged) The memory module of claim 3, wherein the second memory  
2 bus comprises separate address, data, and control signal lines.

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1 5. (Amended) The memory module of claim [1] 3, wherein the second  
2 memory bus comprises a signal line for a clock signal.

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1 6. (Amended) The memory module of claim [1] 3, wherein the first memory  
2 bus operates at a first data rate and the second memory bus operates at a second  
3 data rate, and wherein the first data rate is different than the second data rate.

1 7. (Amended) The memory module of claim 1, wherein the first memory bus  
2 includes [has] a first number of [signals] signal lines and the second memory bus  
3 includes [has] a second number of signal lines, and wherein the first number [of  
4 signal lines] is different than the second number [of signal lines].

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1 8. (Amended) The memory module of claim 1, wherein the memory module  
2 controller comprises:  
3 request handling circuitry [structured] configured to receive the first memory  
4 transaction from the first memory bus; and

5 control logic coupled to the request handling circuitry and configured to  
6 [reformatting] reformat the first memory transaction[, the memory module controller  
7 providing] and to provide the reformatted first memory transaction to at least one of  
8 the plurality of memory devices.

1 9. (Amended) The memory module of claim 1, wherein the first memory bus  
2 [carries] is configured to carry time-multiplexed data and address information, and  
3 the second memory bus includes separate address and data lines.

1 10. (Unchanged) The memory module of claim 1, wherein the memory module  
2 is a dual in-line first memory module (DIMM).

1 11. (Unchanged) The memory module of claim 1, wherein the memory module  
2 is a single in-line first memory module (SIMM).

1 12. (Unchanged) The memory module of claim 1, wherein the plurality of  
2 memory devices comprise volatile memory devices.

1 13. (Unchanged) The memory module of claim 1, wherein the plurality of  
2 memory devices comprise nonvolatile memory devices.

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14. (Amended) The memory module of claim 1, wherein the memory module  
controller is configured to generate [generates] a handshake signal that indicates

3 when the memory module controller is communicating data to the system memory  
4 controller.

1 15. (Amended) The memory module of claim 1, wherein the first memory  
2 transaction is a write transaction.

1 16. (Amended) The memory module of claim 1, wherein the first memory  
2 transaction is a read transaction.

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1 17. (Amended) A memory module comprising:  
2 a plurality of memory devices; and  
3 a memory module controller coupled to [a] the plurality of memory devices,  
4 [wherein] the memory module controller being configured to receive [receives] a  
5 first memory transaction in a first format from [the] a memory bus [in a first format],  
6 and to convert the first memory transaction into a second memory transaction in a  
7 second format, and to provide [provides a] the second memory transaction in [a]  
8 the second format to at least one of the [second] plurality of memory devices.